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Design and Analysis of a Low-Power Full Adder in 90-nm CMOS Technology

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Abstract: Full adders serve as fundamental building blocks within arithmetic units and digital processing cores. In this paper, the authors present the design and transistor level optimization of a full adder using the static CMOS approach within 90nm technology. Special emphasis is placed on transistor sizing techniques to achieve low power consumption. The authors also compared the design with alternative design methodologies such as Complementary Pass Transistor Logic (CPL) and Transmission Gate Adder (TGA) to establish performance baselines. The final design was simulated and validated in Cadence Virtuoso. The results demonstrate improvements in power and delay, as well as area efficiency suitable for large scale VLSI integration. In addition, the importance of choosing appropriate transistor sizing to manage parasitic capacitance and switching energy is emphasized, ensuring a well optimized and technology compatible design. Furthermore, the comparative study helps to understand trade-offs among different full adder architectures. The results of this research reinforce the relevance of full custom design practices even in modern scaled technologies. This implementation is suited for arithmetic intensive applications in DSP and embedded systems. Its simplicity also enables for easier porting to future process nodes, maintaining design flexibility and reusability.

Keywords: *CMOS, Full Adder, Low Power, Transistor Sizing, Cadence Virtuoso.*

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I. INTRODUCTION

Full adders play a pivotal role in digital systems, forming the essential computational units in Arithmetic Logic Units (ALUs), multipliers, and signal processing blocks. As the demand for faster and power-efficient digital hardware grows, optimizing these fundamental components becomes increasingly important.

With scaling into deep sub-micron regimes like 90-nm, parasitic effects, short channel phenomena, and power leakage present notable challenges. In such scenarios, careful circuit-level design, particularly of full adders, can yield substantial gains in power and speed. This paper focuses on designing an efficient full adder circuit using the static CMOS methodology which is shown in Fig. 1 [1]. The authors incorporate strategic transistor sizing to ensure less power consumption while maintaining layout compactness and design rule compliance.

The increased transistor count in full adders also affects the chip area and power consumption, necessitating smart layout decisions. The present work focuses on creating a design that is not only functionally correct but also scalable, robust, and optimized for both layout and performance. As full adders remain an essential part of all digital designs, the improvements here reflect across an entire SoC. Therefore, optimization at this stage has system-level advantages.

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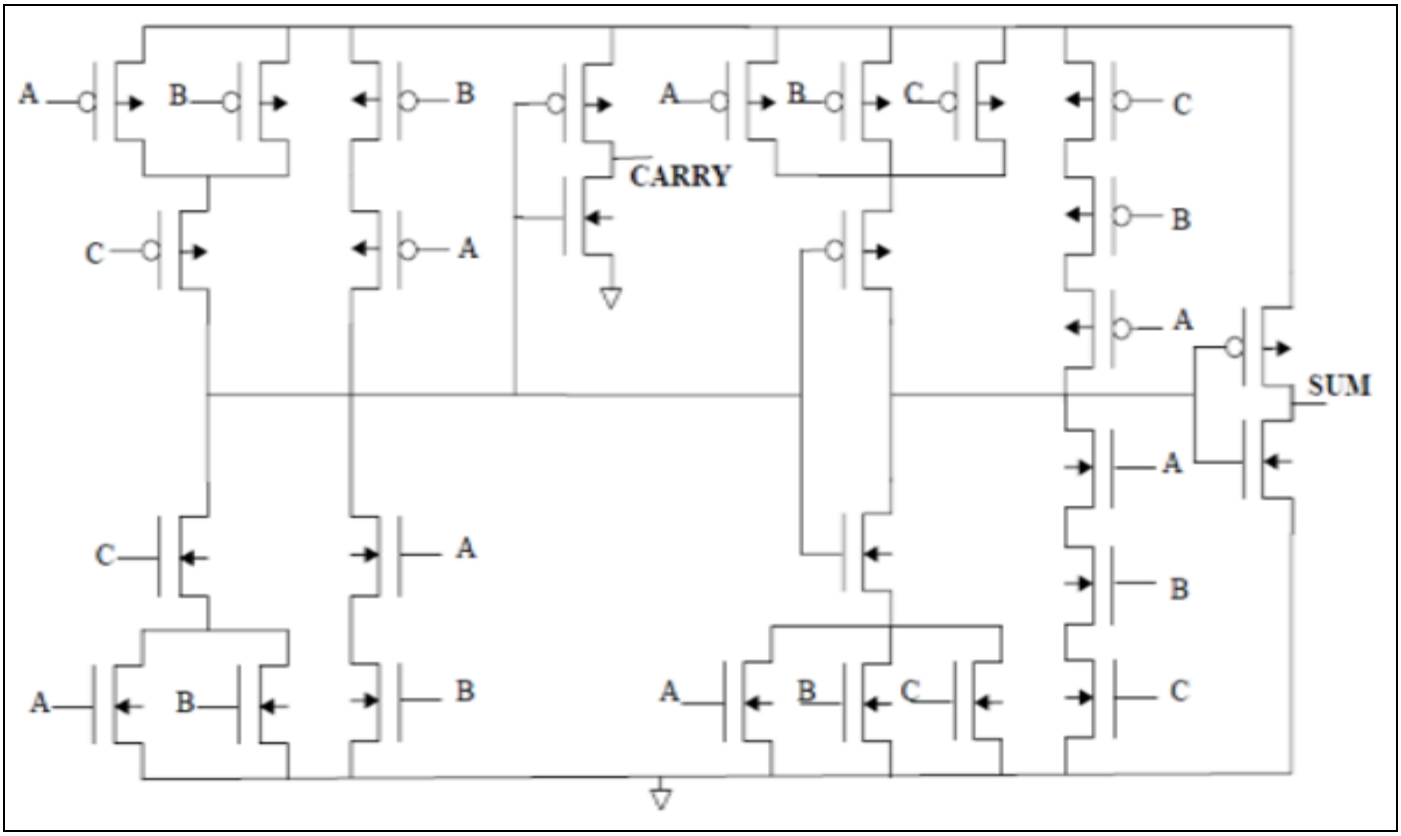

Fig 1 Full Adder circuit using the static CMOS methodology

II. LITERATURE REVIEW

Significant research has been done in the development of efficient full adder architectures. Hybrid logic styles combining Static CMOS with Transmission Gate Logic or Pass Transistor Logic have been explored to minimize transistor count and PDP. In [2], a hybrid 1-bit full adder achieved low power through logic level compression. However, it suffered from poor driving capability and limited noise margins.

The work in [3], [4] emphasizes the importance of technology scaling, particularly in 90nm and below, to ensure compatibility with contemporary fabrication processes. Inverter performance is also significantly influenced by MOSFET parameters such as threshold voltage and channel modulation effects, which impact switching speed and overall efficiency [5]. Additional research highlights the necessity of optimized inverter sizing techniques to mitigate the Miller effect and avoid delay degradation in high-speed applications [6]. These findings underscore the importance of transistor-level optimization and robust simulation during design.

Despite innovations in logic compression and hybridization, Static CMOS still offers superior robustness, noise immunity, and ease of layout verification, which are critical in production-grade designs. The authors' work aims to quantify delay-power tradeoffs across different logic families in a consistent technology node. The review provides insight into the evolution of adder design and helps justify the selection of design methodology in this work. The lessons learned from previous approaches directly influenced the sizing strategies and circuit topologies.

III. METHODOLOGY

➢ *The Proposed Design was Implemented using the Cadence Virtuoso Design Suite. The Complete Workflow Consisted of:*

- **Design Specification:** The authors set performance targets prioritizing low power and low propagation delay.
- **Transistor-Level Schematic:** Manual design and sizing of PMOS/NMOS transistors were carried out to ensure optimal rise/fall symmetry and minimum switching energy.
- **Simulation:** Static and transient simulations were performed under typical process-voltage-temperature (PVT) conditions using the Spectre simulator. Supply voltage was set to 1V.
- **Layout and DRC/LVS:** Layouts were drawn manually, adhering strictly to DRC rules. Layout-vs-Schematic (LVS) checks were performed to confirm consistency with the schematics.
- **Parasitic Extraction:** Parasitic-aware simulations were run to evaluate parasitic capacitance in the circuit.

IV. RESULT AND DISCUSSION

The results of the simulation and analysis on the inverter cell showcased the optimal transistor sizing for efficient switching characteristics which is utilized in the full adder.

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A. Inverter Result

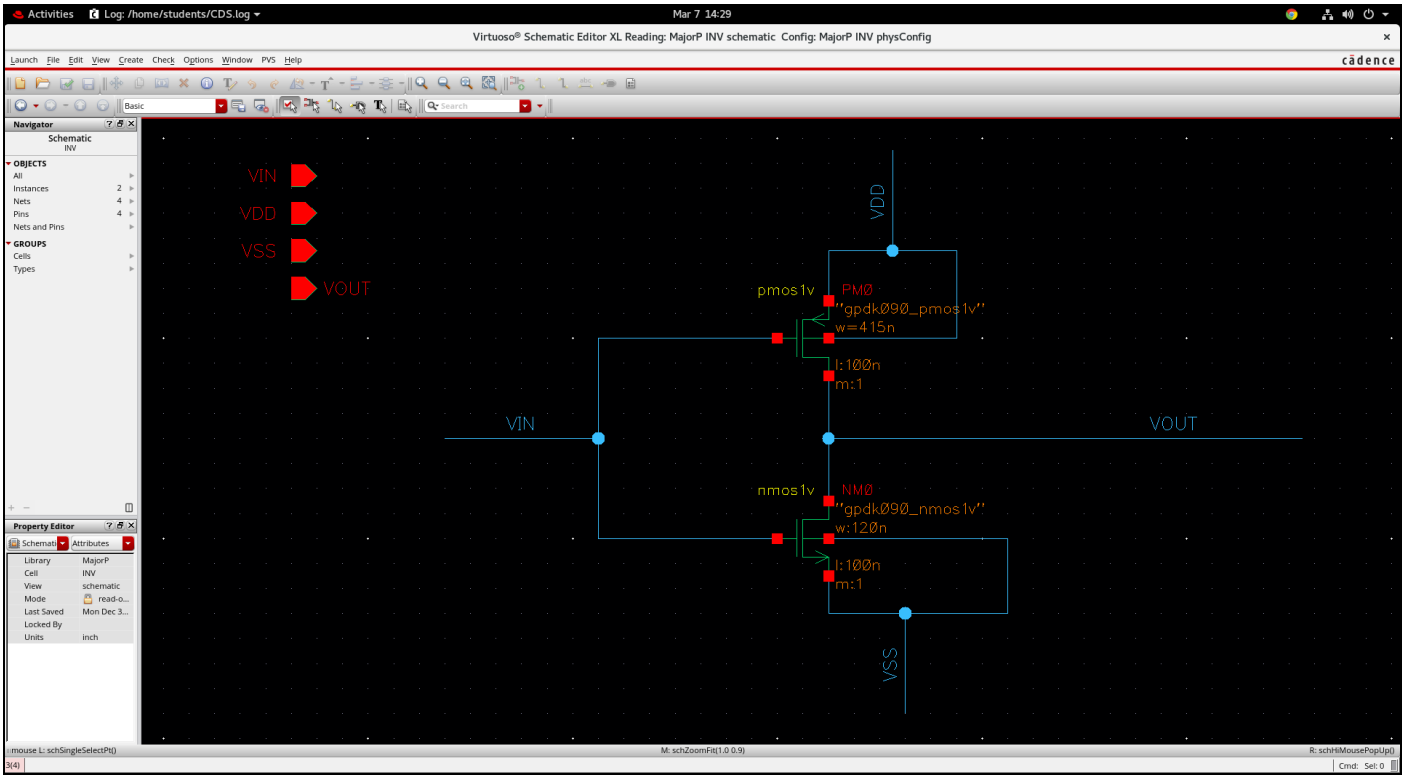

Fig 2 Schematic of the Inverter

Fig. 2, illustrates the schematic of CMOS inverter design in cadence virtuoso using the 90nm technology node. This circuit provides a logic inversion of the input.

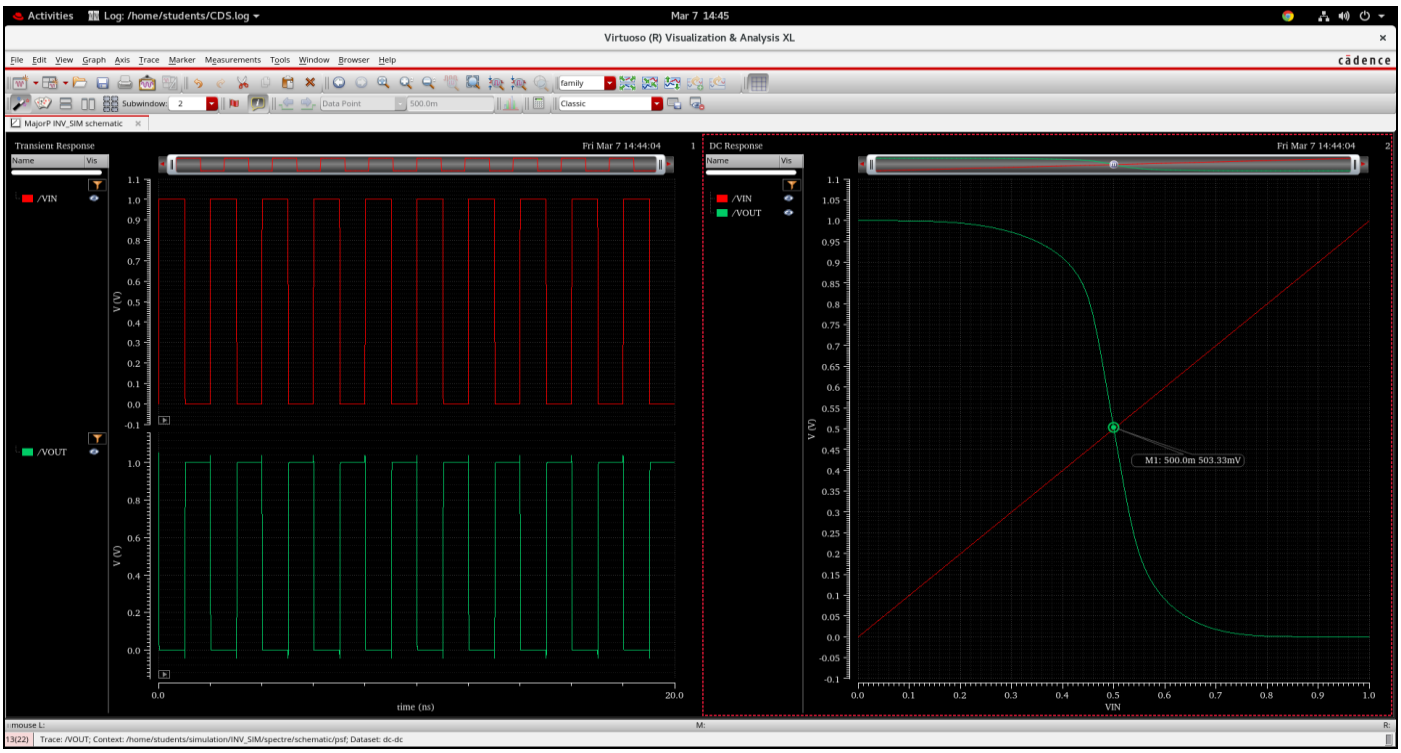

Fig 3 Static and Transient Response of the Inverter

Fig. 3, illustrates the static and transient response of the inverter. The transient response clearly demonstrates proper inversion of the signal provided at the input. The static response i.e. dc analysis shows the Voltage Transfer Characteristics (VTC) of the inverter.

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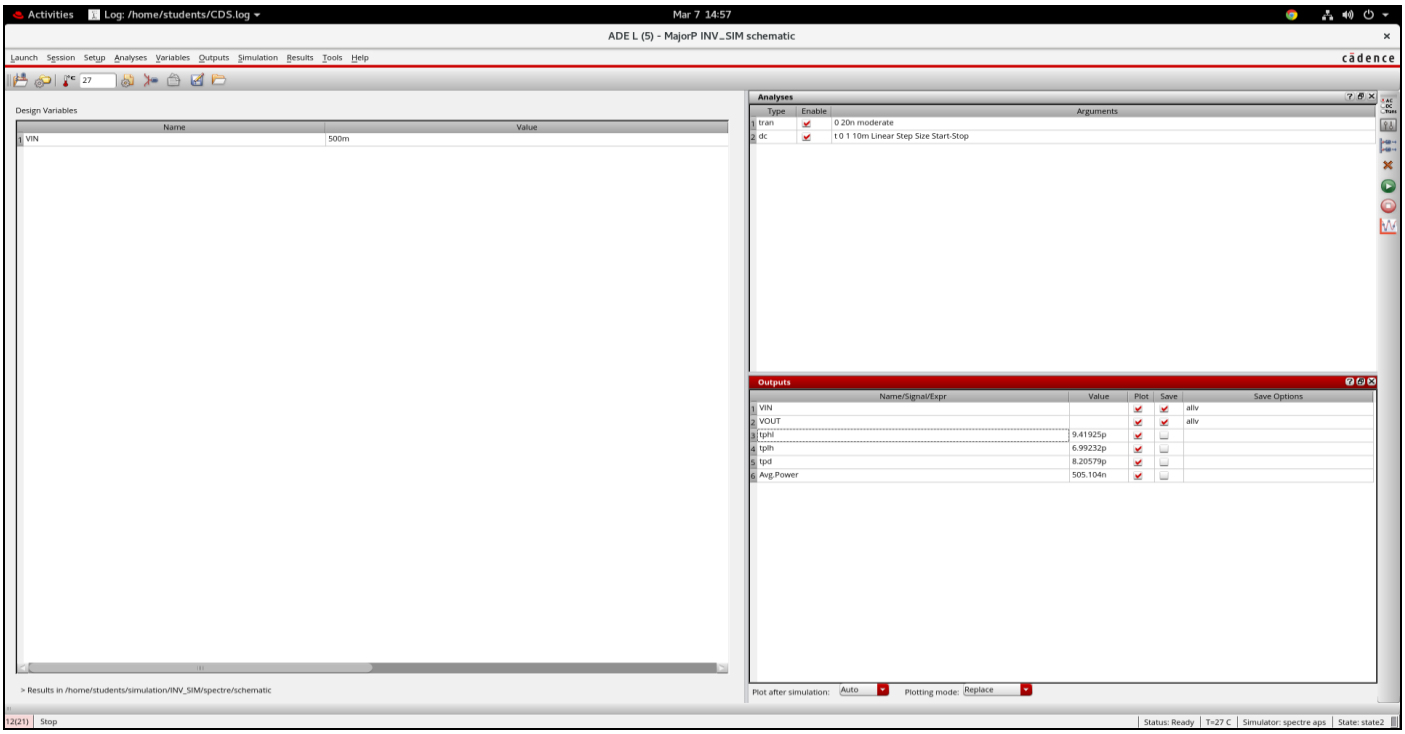

Fig 4 Performance Parameters of the Inverter

Table 1 Performance Parameters of the Inverter

Parameters	Value
tphl	9.41925 ps
tplh	6.99232 ps
tpd	8.20579 ps
Average Power	505.104 nW

Fig. 4, shows the average power and the average delay of the inverter which are clearly mentioned in the Table. 1.

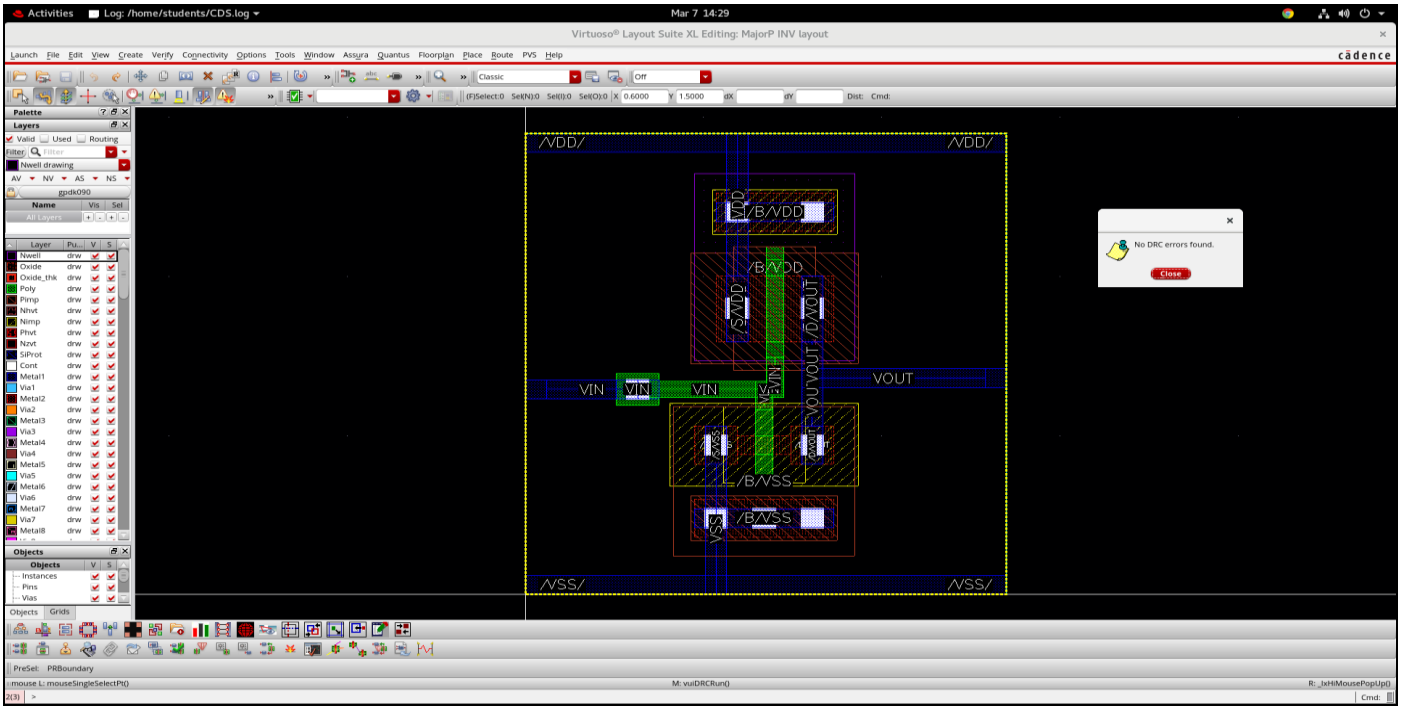

Fig 5 Layout and DRC of the Inverter

Fig. 5, illustrates the inverter layout and shows that the layout is in compliance with all the design rules.

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B. Full Adder Result

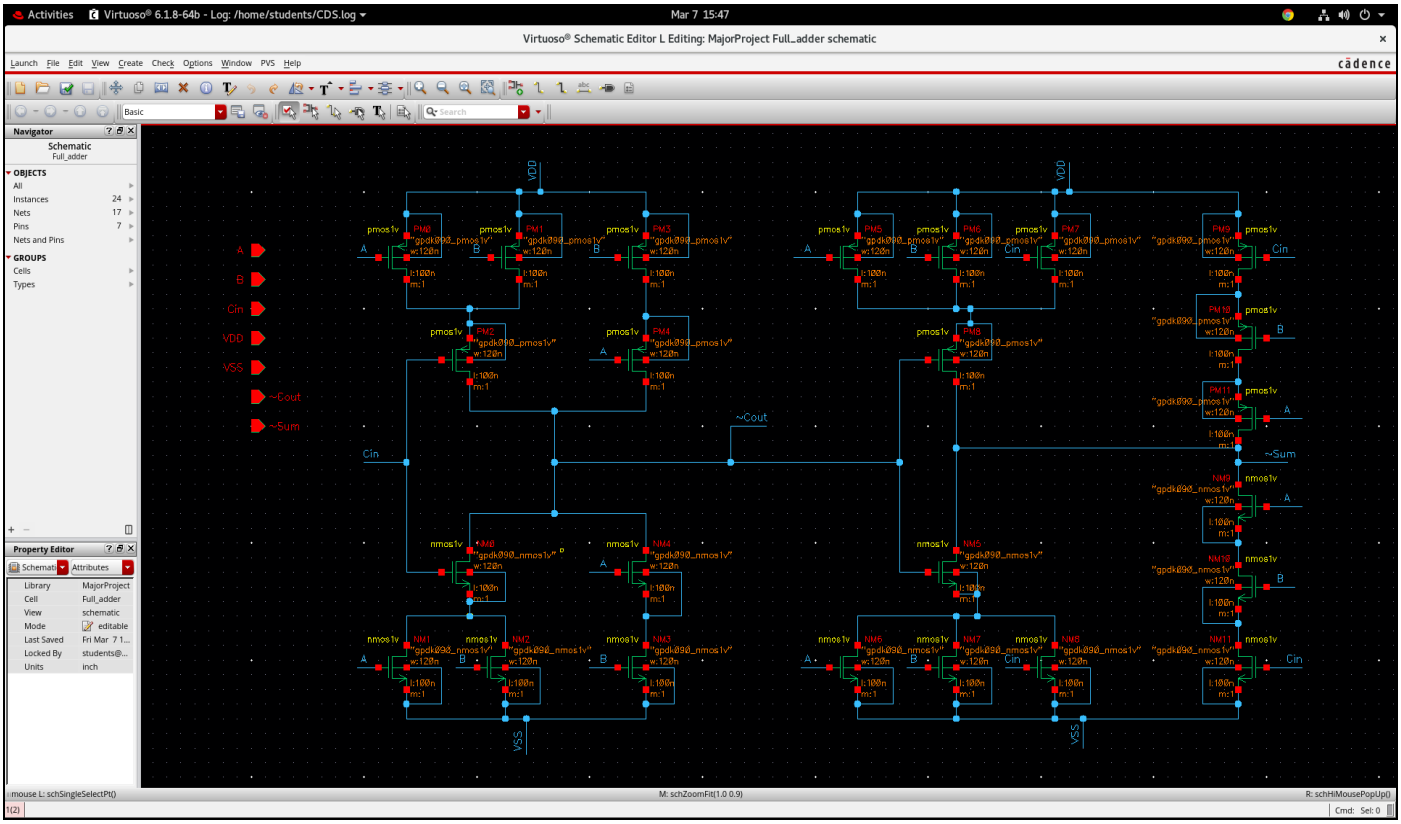

Fig 6 Full Adder Schematic

Fig. 6, shows the schematic of the static CMOS full adder circuit in cadence virtuoso using the 90nm technology node. It has three inputs, i.e. A, B, Cin and two outputs i.e. ~sum and ~cout.

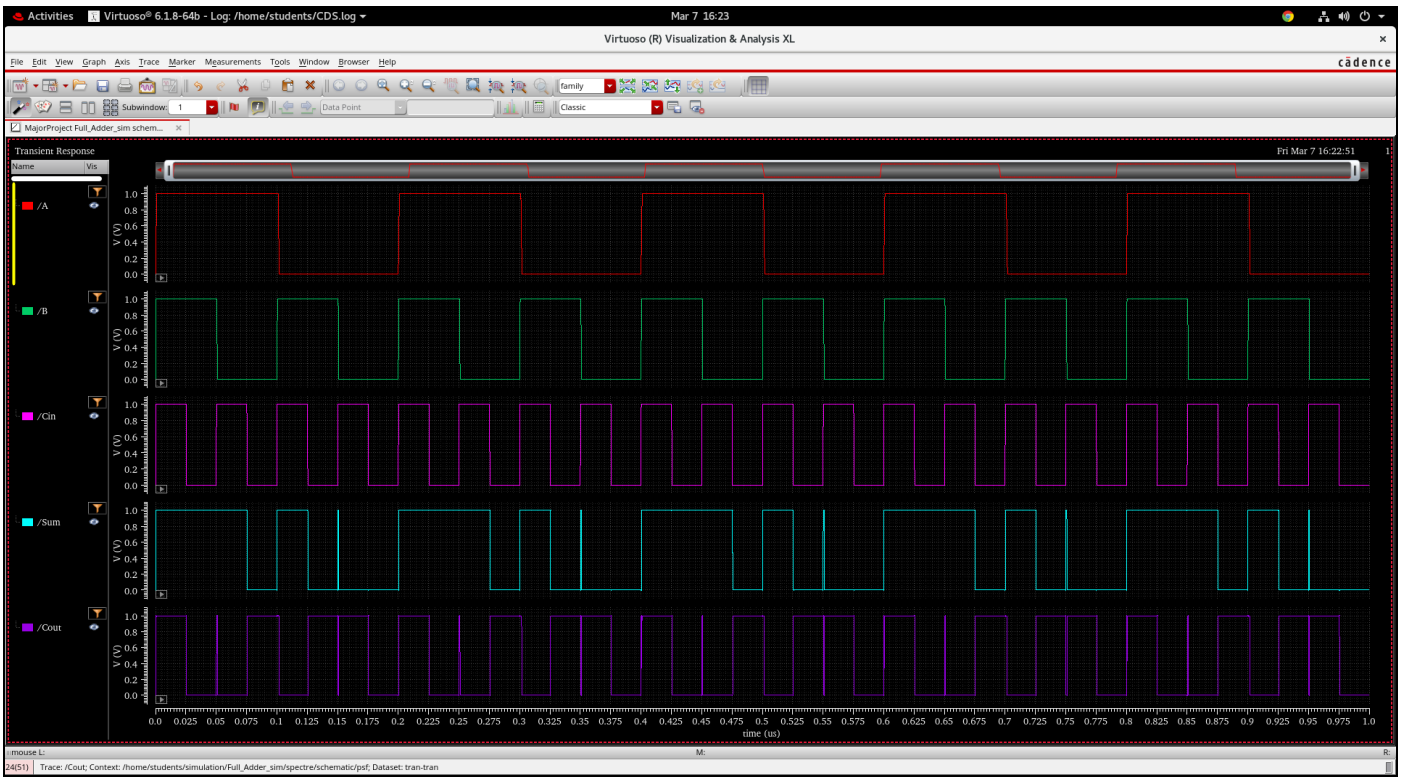

Fig 7 Transient Analysis of Full Adder

The waveform shown in Fig. 7, shows the output of the full adder with respect to the input provided.

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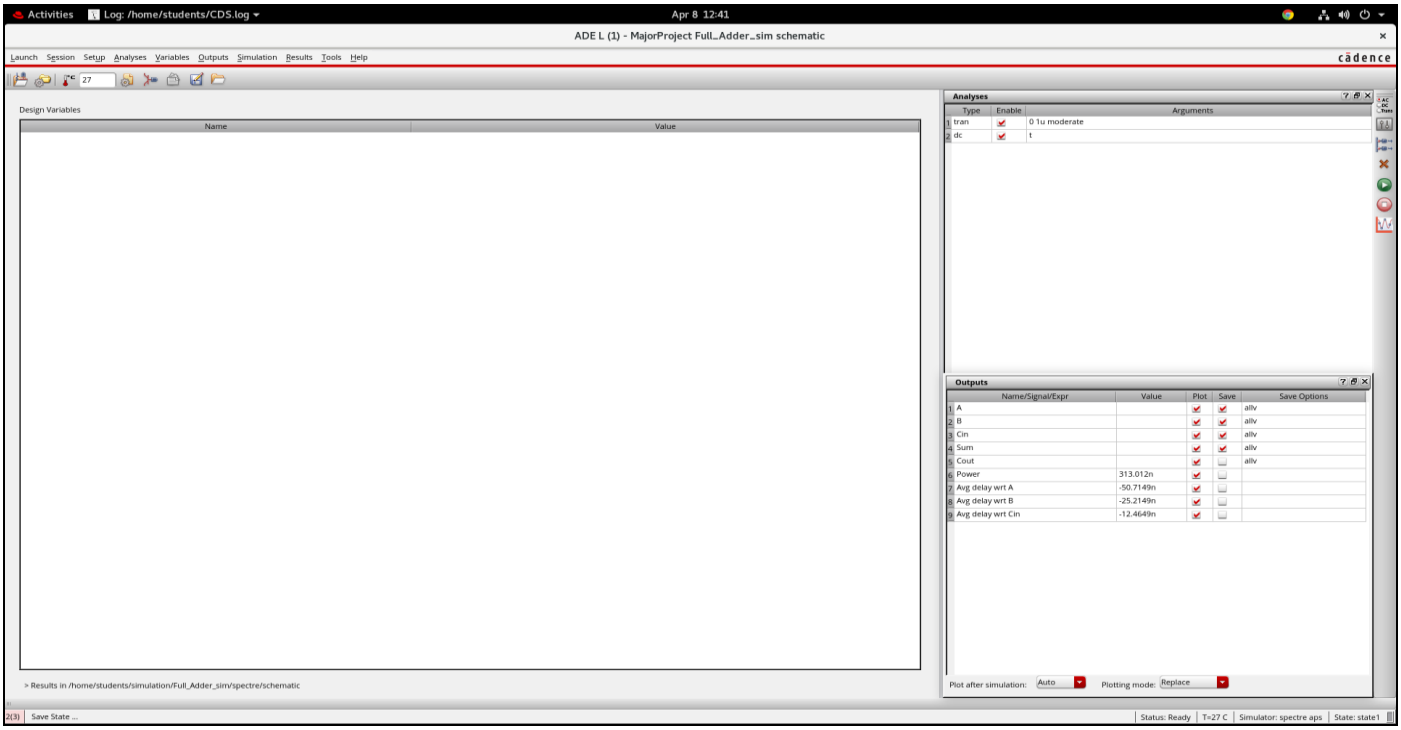

Fig 8 Performance Parameters of Full Adder

Table 2 Performance Parameters of the Inverter

Parameters	Value
Average Power	0.313 µW

Fig. 8, shows the average power consumption of the full adder which is displayed in Table 2.

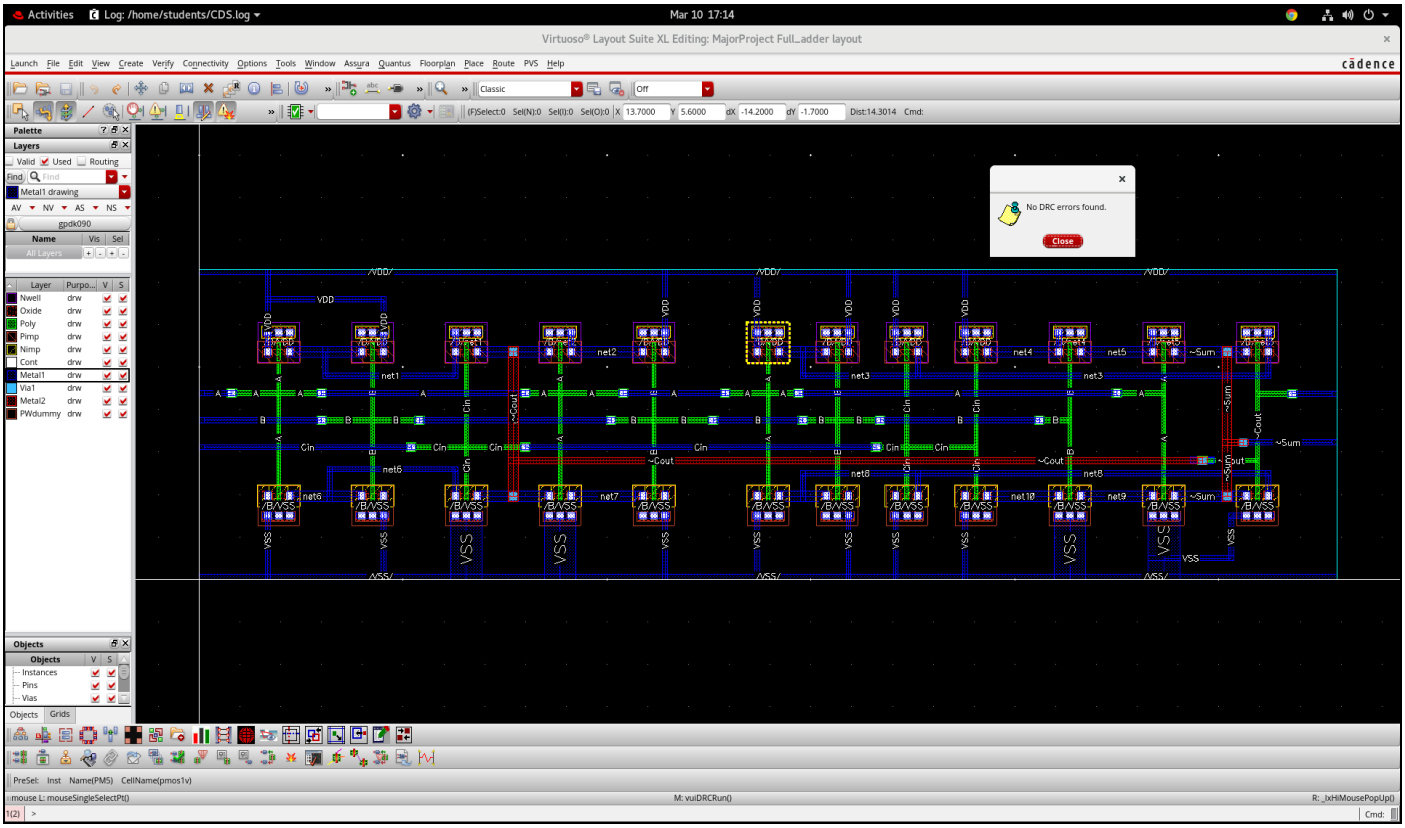

Fig 9 Layout and DRC of the Full Adder

Fig. 9, illustrates the full adder layout and shows that the layout is in compliance with all the design rules.

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Table 3 Comparative Analysis of Power Consumption by Different Design Style

Design Style	**Power (**µW)
Hybrid A	1.61
Hybrid B	0.67
CPL	1.7598
TGA	1.7619

Table 3, indicates the power consumed by different design styles [7]. It concludes that the power consumption of the proposed design shows significant upper hand.

V. CONCLUSION

A low power full adder was successfully designed using 90nm Static CMOS. By leveraging strategic transistor sizing and thorough layout validation, we achieved a significant improvement in power consumption. Simulation and analysis confirm its suitability for integration in modern digital VLSI systems.

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